Using a Negative Capacitance to Increase the Tuning Range of a Varactor Diode in MMIC Technology

Svilen Kolev*, Member, IEEE, Bruno Delacressonnière**, Member, IEEE,
Jean-Luc Gautier**, Senior Member, IEEE

* Corning Inc., European Research Center, 77210 Avon, France
** ENSEA-EMO, 95014 Cergy-Pontoise, France

***Abstract* — An original method to increase the tuning range of a MMIC varactor diode is presented. An active circuit simulating a negative capacitance is connected to the varactor diode. This method allows to increase the varactor's tuning range more than ten times. A MMIC simulating a negative capacitance have been successfully fabricated and measured and we hope to be able to present measured results of a complete active varactor by the time of the symposium.**

I. Introduction

The main difficulties in the design of tunable active circuits in MMIC HEMT technology are due to the insufficient performances of the tunable elements. Tunable active filters and voltage controlled oscillators (VCO) most often employ varactor diodes in their structures. In the case of wide-band VCOs, the frequency range covered f_{max}/f_{min} is proportional to the square root of the varactor's tuning range C_{max}/C_{min}. In addition, VCO phase noise strongly depends on the quality factor of the tunable element.

However, in HEMT processes, the varactor diodes are somewhat degenerated, since they are obtained on the basis HEMTs, and the capacitance effect is mainly caused by modulation of the 2DEG. The typical tuning range C_{max}/C_{min} of a MMIC varactor is about 2 to 3 units, if device's series resistance is to be kept reasonable. Typical series resistance of a MMIC varactor varies from several Ohms to several tens of Ohms. In addition, this resistance depends on the device's bias voltage [1].

This paper describes a method to increase the tuning range of varactor diodes in HEMT technology and to compensate at the same time their series resistance by connecting in series an active circuit simulating a negative capacitance.

II. Characteristics of Varactor Diodes in HEMT Technology

Fig.1 presents the performance of a MMIC varactor diode in the 0.2 μm gatelength pHEMT process ED02AH of Philips-PML [1]. This device has a total electrode width of 6x100 μm.

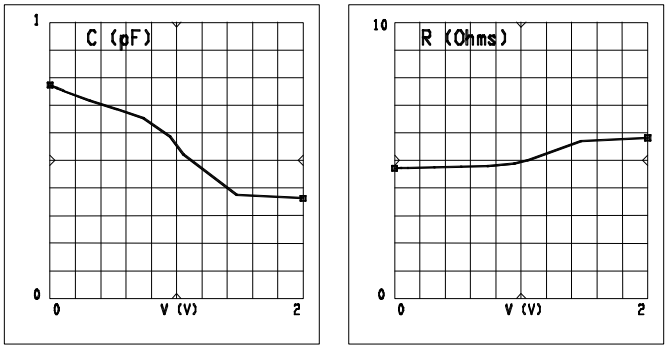

Fig. 1. Tuning characteristics of a DIGM-type 6x100μm Philips varactor in the ED02AH pHEMT process.

The tuning range C_{max}/C_{min} of this device is 2.1 units and its series resistance is about 5 Ω for a reverse bias voltage ranging from 0 to 2 V. There is another type of varactor diodes in the ED02AH process, the DIBE-type, with an electrode length of 3 μm, instead of 0.2 μm. It allows to obtain tuning ranges of about 12 units, but the series resistance is very bias-dependent and can attain several tens of Ohms. If one wishes to limit it, the tuning range is reduced to about 1.5 units, depending on the total width of the device. These tuning range values are similar in all MMIC HEMT processes.

III. Circuit Design and Characterization

A. Principle of Operation

The series association of a negative capacitance (an element whose admittance can be written as Y=-jωC) and a tunable positive capacitance with a tuning range from $\mathbf{C_{min}}$ to $\mathbf{C_{max}}$ is represented in Fig.2.

Fig. 2. Series association of a negative capacitance C_n and a tunable positive capacitance C.

Assuming that these two elements are lossless, the resulting capacitance is :

$$C_{eq} = \frac{CC_n}{C + C_n} \qquad (1)$$

In order to obtain a positive capacitance, we must take $|C_n| > C_{max}$. Let us pose $C_n = -kC_{max}$, where k > 1. According to (1), we then have :

$$C_{eq\max} = \frac{-C_{\max} kC_{\max}}{C_{\max} - kC_{\max}} = \frac{k}{k-1} C_{\max} \quad \text{and}$$

$$C_{eq\min} = \frac{-C_{\min} kC_{\max}}{C_{\min} - kC_{\max}} \qquad (2)$$

If $D = \frac{C_{\max}}{C_{\min}}$ is the tuning dynamics of the positive capacitance C, the tuning dynamics D' of the series association can be written as :

$$D' = \frac{C_{éq\max}}{C_{éq\min}} = \frac{k}{k-1}(D - \frac{1}{k}) \qquad (3)$$

When the coefficient *k* is close to 1, e.g. $|C_n|$ is close to C_{max}, it can be clearly seen that the tuning dynamics of the series association can reach very high values.

B. The Negative Capacitance

This circuit is based on a Negative Impedance Converter, designed with two common-source transistors and loaded with an inductor (Fig.3), [1], [2] :

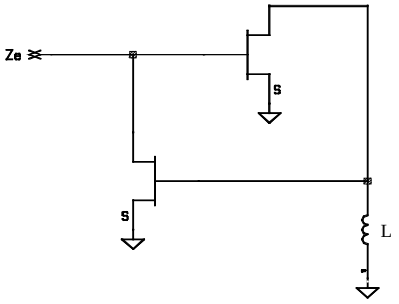

Fig. 3. Principle schematic of the NIC-based Negative Capacitance.

The two Common Source stages form a Negative Impedance Converter, which is loaded with the inductive load L. The equivalent circuit, obtained using a 3-element HEMT model (C_{gs}, g_m, R_{ds}) and supposing that the two transistors are identical, is shown in Fig. 4.

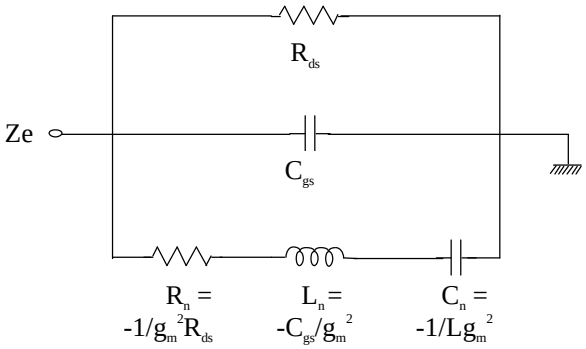

Fig. 4. Equivalent circuit of the negative capacitance.

If the operating frequency is much smaller than the characteristic frequency :

$$f_1 = \frac{g_m^2 R_{ds}}{2\pi C_{gs}} = f_t g_m R_{ds} \approx 16 f_t, \qquad (4)$$

where f_t is the cut-off frequency of the transistors, the influence of the parallel elements is negligible and the equivalent circuit can be reduced to that of Fig.5.
Let us also notice that for a Field-Effect Transistor the product $g_m R_{ds}$ is much greater than 1 and independent of the gatewidth. It is equal to about 16 for a Philips pHEMT of the ED02AH process.

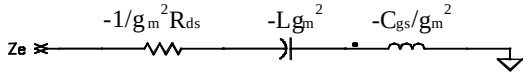

Fig. 5. Simplified equivalent circuit.

This is a series RLC circuit. The negative resistance and the negative inductance can be compensated by placing a resistor and an inductor of proper values at the circuit's input. We thus obtain a negative capacitance of $-Lg_m^2$, where L is the value of the load inductor and g_m^2 is the transconductance of the pHEMTs.

C. Simulation and Measurement Results of the Negative Capacitance

In order to demonstrate the feasibility of a MMIC simulating a negative capacitance, a circuit has been designed and fabricated using the 0.25 μm gatelength pHEMT process H40 of GEC-Marconi. The circuit's photograph is shown in Fig. 6.

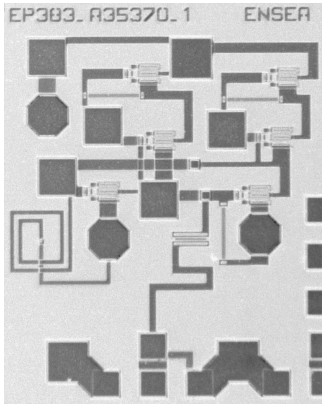

Fig. 6. Photo of the negative capacitance.

The pHEMTs are two-gate finger devices with a total gatewidth of 2x60 μm. They are biased using active loads. At the input, we have placed two compensation elements – an inductor, realized with transmission lines and a resistor, which compensate the circuit's intrinsic negative inductance and negative resistance respectively (Fig.4). We have also placed a parallel capacitor of about 2.6 pF at the input, in order to obtain a total positive capacitance (a negative capacitance alone cannot be measured, because it oscillates). This parallel capacitor is integrated only to be able to measure the circuit; in a real application it will be needless (the negative capacitance will be connected to another sub-circuit, for example a varactor diode). We should however notice that this capacitor and the transmission lines connecting it to ground resonate at about 12 GHz (in our case), thus limiting the circuit's bandwidth. On the same chip we have realized separately the same positive capacitor of 2.6 pF in order to be able to measure it precisely and to extract the negative capacitance. We have also realized on the same chip several test structures: a transistor and an inductor, to be able to estimate the technological variations of the process. The circuit's active surface is 0.8x0.8 mm. Post-layout simulation and measurement results of the complete circuit are shown in Fig. 7.

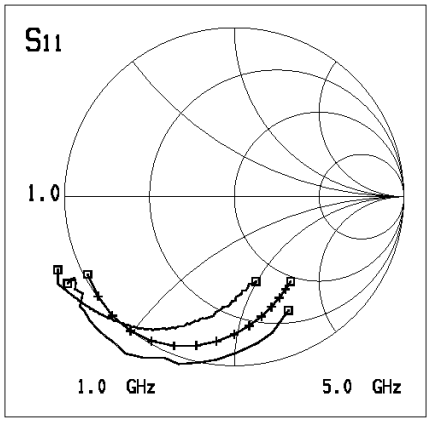

Fig. 7. Post-layout simulation and measurement results of the circuit including the parallel positive capacitor at the input.

The crossed line trace in the middle shows the post lay-out simulated S_{11} of the circuit. The inner and the outer traces represent the measured S_{11} at V_{DD}= 4V and 9V respectively. The negative resistance observed is due to the technological variations of the transconductance g_m of the transistors. Let us remind that the circuit's intrinsic negative resistance (Fig.4) is equal to $-1/g_m^2R_{ds}$. The test transistors manufactured separately on the same chip showed variations of g_m as high as 20%, which are typical to the H40 [1]. Using a more precise process allows to obtain a virtually pure negative capacitance in a much larger bandwidth (0.2-12 GHz) [1]. The extracted negative capacitance is shown in Fig. 8.

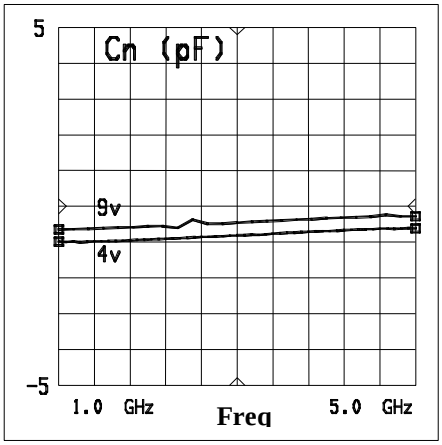

Fig. 8. Extracted negative capacitance at V_{DD} = 4V et 9V.

We obtain a negative capacitance of about – 1pF at V_{DD}=4V. The compensation of the negative inductance turns out to be incomplete, because its value has been modified by the technological variation of g_m during processing.

D. Series Association of a Negative Capacitance and a Varactor Diode

Fig. 9. shows the schematic of the circuit. The varactor diode D is biased via two high-value resistors, R_1 et R_2.

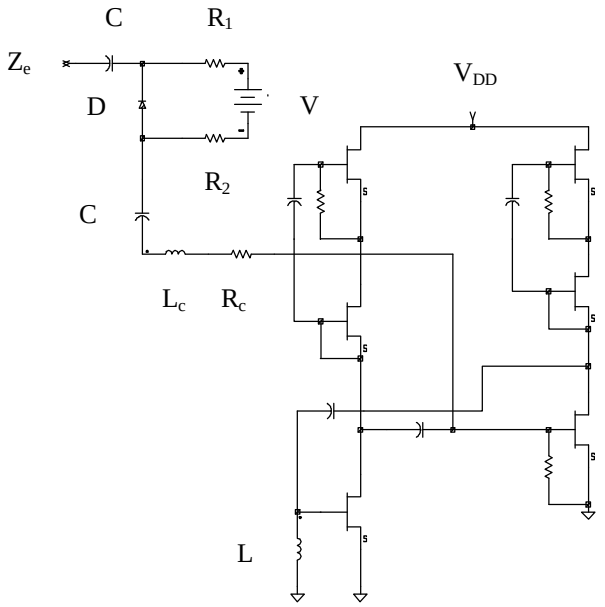

Fig. 9. Series association of a negative capacitance and a varactor diode.

All pHEMT are 2x50 µm devices. The negative capacitance is equal to –0.8 pF. The circuit's intrinsic negative resistance R_n (see the equivalent circuit of Fig. 4) is about –10 Ω. The compensation resistor R_c is chosen 5.8 Ω, the compensation inductor L_c (realized with a transmission line) is equal to 0.16 nH so we obtain a series RC circuit with C = -0.8 pF and R = - 4.2 Ω. The negative resistance that results compensates the series resistance of the varactor diode. It can also be shown [1] that the resonant frequency of the series association is reduced

$\sqrt{\frac{k}{k-1}}$ times approximately compared to the resonant frequency of the varactor diode alone. The resonant frequency of the series association in this case is 7.5 GHz. The simulation results (MDS) with the compete foundry models of all elements, taking into account their parasitics, are shown in Fig. 10.

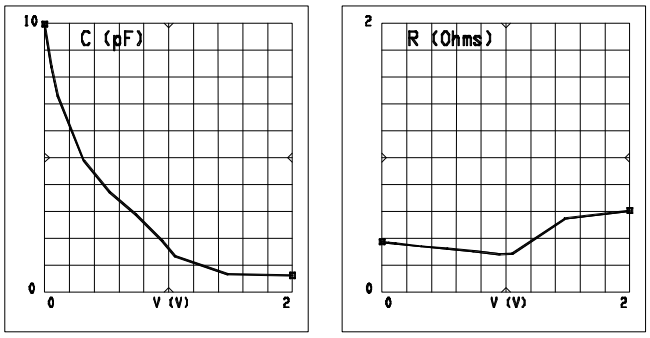

Fig. 10. Series association : simulation results at 2 GHz with the complete foundry models of all elements.

The capacitance is varying from 10 pF to 0.62 pF for a reverse bias voltage of the varactor diode ranging from 0 to 2 V. Thus, the tuning range $\mathbf{C_{max}/C_{min}}$ of this series association is 16 units and its series resistance is about 0.4 Ω. We have been able to increase about 8 times the tuning range of the varactor diode and to compensate its series resistance at the same time.

IV. Conclusion

An original method to increase the tuning range of MMIC varactor diodes has been presented. A negative capacitance has been used. The feasibility of a negative capacitance in MMIC technology has been demonstrated and the authors hope to present measurement results of the complete "active" varactor by the time of the symposium. To the best of our knowledge this is the first time that the feasibility of "active" varactors has been investigated.

Acknowledgement

The authors wish to thank Prof. Daniel Pasquet for performing the measurements and for useful discussions.

References

[1] S. Kolev "Design of Active Circuits Simulating Tunable Capacitances with Wide Tuning Range in MMIC Technology", *Ph.D. Thesis, University of Paris VI*, France, July 2000

[2] S. Kolev, B. Delacressonnière, J.-L. Gautier, "Novel Microwave Negative Capacitance. Application to a Wide-Range Tunable Capacitance" *30rd European Microwave Conference Proceedings*, Paris, 2000

[3] S. Susman-Fort, L. Billonnet, "A NIC-Based Negative Capacitance Circuit for Microwave Active Filters", International Journal of Microwave and Millimeter - Wave Computer - Aided Engineering, 1995, vol.5, n°4